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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously presented): An apparatus for suppressing limit cycles during noise conversion, comprising:

a filter block for noise conversion, said filter block for obtaining an input signal, said filter block for providing a signal;

an adder having a first input and a second input, said first input of said adder obtaining the signal from said filter block and said second input of said adder obtaining a feedback signal, said adder for providing an output signal;

a divider stage for converting the output signal from said adder into a digital signal including n bits and into an error signal; and

a feedback block for generating the feedback signal from the error signal, said feedback block including a sign converter for determining a positive value of the error signal and a time delay element.

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Claim 2 (original): The apparatus according to claim 1,
wherein said filter block is designed as a two-stage noise
shaping filter or as a three-stage noise shaping filter.

Claim 3 (canceled)

Claim 4 (previously presented): An apparatus for suppressing
limit cycles during noise conversion, comprising:

a filter block for noise conversion, said filter block for
obtaining an input signal, said filter block for providing a
signal;

an adder having a first input and a second input, said first
input of said adder obtaining the signal from said filter
block and said second input of said adder obtaining a feedback
signal, said adder for providing an output signal;

a divider stage for converting the output signal from said
adder into a digital signal including n bits and into an error
signal;

a feedback block for generating the feedback signal from the
error signal;

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said feedback block including a sign converter for determining a positive value of the error signal; and

said feedback block further including a filter element having a transfer function $\frac{1}{z+\alpha}$, where $\alpha = 2^{-s}$, and s is a natural number.

Claim 5 (previously presented): An apparatus for suppressing limit cycles during noise conversion, comprising:

a filter block for noise conversion, said filter block for obtaining an input signal, said filter block for providing a signal;

an adder having a first input and a second input, said first input of said adder obtaining the signal from said filter block and said second input of said adder obtaining a feedback signal, said adder for providing an output signal;

a divider stage for converting the output signal from said adder into a digital signal including n bits and into an error signal;

a feedback block for generating the feedback signal from the error signal

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said filter block is a digital filter; and

said adder, said divider stage and said feedback block are implemented as digital signal processing stages.

Claim 6 (original): The apparatus according to claim 5, wherein said divider stage provides the error signal as a digital error signal including m bits.

Claim 7 (original): The apparatus according to claim 5, wherein said feedback block includes a sign converter for determining a magnitude of the error signal.

Claim 8 (original): The apparatus according to claim 5, wherein said feedback block includes a sign converter for determining a two's complement of the error signal.

Claim 9 (original): The apparatus according to claim 5, wherein:

said feedback block includes a filter element having a transfer function $\frac{1}{z+\alpha}$, where $\alpha = 2^{-s}$, and s is a natural number;

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said filter element is implemented by a time delay element providing an output signal, said time delay element obtains an input signal; and

the output signal of said time delay element, shifted to the right by s bit positions, is subtracted from the input signal of said time delay element.

Claim 10 (original): The apparatus according to claim 5, wherein when said feedback block generates the feedback signal using a calculation with an accuracy that is increased by at least one additional less significant bit.

Claim 11 (original): The apparatus according to claim 5, wherein said filter block, said adder, said divider stage, and said feedback block are implemented with a digital signal processor.

Claim 12 (original): The apparatus according to claim 5, wherein said filter block, said adder, said divider stage, and said feedback block are implemented as a hardware circuit configuration.

Claim 13 (original): The apparatus according to claim 5, wherein the input signal provided to said filter block is a

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digitized audio signal being processed in a mobile radio receiver.

Claim 14 (original): The apparatus according to claim 1, wherein:

said filter block is an analog filter; and

said adder and said feedback block are implemented as analog signal processing stages.

Claim 15 (original): The apparatus according to claim 14, wherein:

said divider stage includes an initial stage with an analog/digital converter for generating the digital signal including n bits.

Claim 16 (previously presented): An apparatus for suppressing limit cycles during noise conversion, comprising:

an analog filter block for noise conversion, said analog filter block for obtaining an input signal, said analog filter block for providing a signal;

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an adder, implemented as an analog signal processing stage, having a first input and a second input, said first input of said adder obtaining the signal from said analog filter block and said second input of said adder obtaining a feedback signal, said adder for providing an output signal;

a divider stage for converting the output signal from said adder into a digital signal including n bits and into an error signal;

a feedback block, implemented as an analog signal processing stage, for generating the feedback signal from the error signal;

the digital signal of said divider stage is converted back into an analog signal;

the output signal of said adder is an analog output signal;
and

the analog signal of said divider stage and the analog output signal of said adder are used to produce the error signal as an analog error signal.

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Claim 17 (original): The apparatus according to claim 14, wherein said adder is implemented using an operational amplifier.

Claim 18 (previously presented): An apparatus for suppressing limit cycles during noise conversion, comprising:

an analog filter block for noise conversion, said analog filter block for obtaining an input signal, said analog filter block for providing a signal;

an adder, implemented as an analog signal processing stage, having a first input and a second input, said first input of said adder obtaining the signal from said analog filter block and said second input of said adder obtaining a feedback signal, said adder for providing an output signal;

a divider stage for converting the output signal from said adder into a digital signal including n bits and into an error signal;

a feedback block, implemented as an analog signal processing stage, for generating the feedback signal from the error signal;

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said feedback block includes a sign converter for determining
a positive value of the error signal; and

said sign converter is implemented using a rectifier.

Claim 19 (original): The apparatus according to claim 14,
wherein said analog signal processing stages are implemented
using switched capacitor technology.

Claim 20 (original): The apparatus according to claim 14,
wherein the input signal provided to said filter block is
obtained from an analog signal that will be digitally
recorded.

Claim 21 (currently amended): A method for suppressing limit
cycles during noise conversion, the method which comprises:

obtaining a resultant signal by using a filter block for noise
conversion to filter an input signal;

obtaining an output signal by adding a feedback signal to the
resultant signal of the filter block;

converting the output signal into a digital signal including n
bits and into an error signal; ~~and~~

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generating the feedback signal starting from the error signal by determining a positive value of the error signal, and filtering the positive value of the error signal using a filter element having a filter characteristic $\frac{1}{z+\alpha}$, where $\alpha = 2^{-s}$, and s is a natural number; and

outputting the content of the digital signal to a user.

Claim 22 (original): The method according to claim 21, which further comprises:

performing the step of generating the feedback signal by determining a positive value of the error signal and storing the positive value of the error signal in a time delay element.

Claim 23 (canceled)

Claim 24 (original): The method according to claim 21, which further comprises:

using digital processing stages to perform the steps of obtaining a resultant signal, obtaining an output signal,

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converting the output signal, and generating the feedback signal.

Claim 25 (original): The method according to claim 24, which further comprises:

converting the output signal, obtained by adding the feedback signal to the resultant signal of the filter block, into a digital signal including n bits and into a digital error signal including m bits.

Claim 26 (currently amended): A method for suppressing limit cycles during noise conversion, the method which comprises:

obtaining a resultant signal by using a filter block for noise conversion to filter an input signal;

obtaining an output signal by adding a feedback signal to the resultant signal of the filter block;

converting the output signal into a digital signal including n bits and into an error signal;

generating the feedback signal starting from the error signal;

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using digital processing stages to perform the steps of
obtaining a resultant signal, obtaining an output signal,
converting the output signal, and generating the feedback
signal;

performing the step of generating the feedback signal by
determining a positive value of the error signal, and
filtering the positive value of the error signal using a
filter element having a filter characteristic $\frac{1}{z+\alpha}$, where $\alpha = 2^{-s}$, and s is a natural number;

implementing the filter element with a time delay element
providing an output signal; and

shifting the output signal of the time delay element to the
right by s bit positions and each time the output signal is
shifted to the right by s bit positions, subtracting the
output signal of the time delay element from the input signal
of the time delay element; and

outputting the content of the digital signal to a user.

Claim 27 (original): The method according to claim 21, which
further comprises:

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using analog processing stages to perform the steps of obtaining a resultant signal, obtaining an output signal, converting the output signal, and generating the feedback signal.

Claim 28 (original): The method according to claim 27, which further comprises:

converting the output signal, obtained by adding the feedback signal to the resultant signal of the filter block, into a digital signal including n bits.

Claim 29 (original): The method according to claim 27, which further comprises:

converting the digital signal back into an analog signal;

providing the output signal, being obtained by the adding, as an analog output signal; and

producing the error signal as an analog error signal obtained from the analog output signal and the analog signal converted from the digital signal.

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Claim 30 (previously presented): The method of claim 21,
including the further step of outputting the output signal.

Claim 31 (previously presented): The method of claim 26,
including the further step of outputting the output signal.